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EXAMINER	
GEBRESILASSIE, KIBROM K	

ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/693,484	STEVENS ET AL.	
	Examiner	Art Unit	
	KIBROM K. GEBRESILASSIE	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,6-18,21,44,46,48,55-58 and 63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2, 3, 6-18, 21,44, 46, 48, 55-58, and 63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amended application filed on 06/05/2008.

2. Claims 2, 3, 6-18, 21, 44, 46, 48, 55-58, and 63 are presented for examination.

3. Claims 1, 4, 5, 19, 20, 22-43, 45, 47, and 49-54 have been canceled.

Response to Arguments

4. Applicants are thanked for amendment/Remarks.

5. Applicant's amendment relating to Objection to the Specification is **considered and is entered**.

6. Applicant's amendment relating to Claim Objection is persuasive and therefore the objection is **withdrawn**.

7. Double Patenting rejection is **maintained** until Terminal Disclaimer is provided.

8. Applicant's amendment relating to 112 rejection is persuasive and therefore the rejection is **withdrawn.**

9. Applicant's argument relating to 101 rejection, specifically relating to practical application, is not persuasive (See **Claim Rejections - 35 USC § 101 below).**

10. Regarding claims 22, 32, and 39, Applicants are canceled claims 22, 32, and 39 and therefore the 101 rejection is **withdrawn.**

11. Applicant's amendment relating to 101 rejection, specifically being **software per se,** is persuasive and therefore the rejection is **withdrawn**. The claims amended to recite a "computer hardware" that permits the functionality of the software to be realized.

12. Applicant's arguments with respect to the art rejections have been considered but are moot in view of the new ground(s) of rejection.

Priority

13. Acknowledgment is made of applicant's claim for benefit of the filing date of a continuation-in-part of the prior application.

Double Patenting

14. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

15. Claims 2, 12, and 18 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 2, 12, and 16 of U.S. Patent No. 6,678,876. Although the conflicting claims are not identical, they are not patentably distinct from each other because all claims are directed to creating an initial array of nodes within a routing space, adjusting initial array of nodes, and selecting a path through adjusted array of nodes. Claims 2, 12, and 16 of Patent No. 6,678,876 contain every element of claims 2, 12, and 18 of the instant application and anticipate the claims of the instant application. Claims of the instant application are not patently distinct from the earlier patent claims and as such are unpatentable over obvious-type double patenting. A later application claim is not patentably distinct from an earlier claim if the later claim is anticipated by the earlier claim.

Claim Rejections - 35 USC § 101

16. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

17. Claims 2, 3, 6-18, 21, 44, 46, 48, 55-58, and 63 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter since the claims as a whole do not provide for a practical application that produce a useful, tangible and concrete result. The independent claims recite "selecting a path" resulting in creation of a trace, which only refers to a **decision** and no tangible result, and thus no practical application is produced. This is not the kind of real-world application that has been held to be a useful, concrete, and tangible result. Claims as a whole produce no tangible result.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

19. Claims 2, 3, 6-18, 21, 44, 46, 48, 55-58, and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Publication No. 2001/0038612 issued to Vaughn et al in view of Patent No. 7, 065, 729 issued to Chapman et al.

20. As per Claim 1, Canceled.

21. As per claim 2, Vaughn et al discloses a computer comprising computer hardware system for use in generating paths finding a path for electrically conductive traces-within a routing space comprising:

means for creating an initial array of nodes within the routing space proposed physical layout (such as *…the routing path data from the optimized segments file created by the analysis engine and redefines the path segments in terms of coordinates*

...the end result of the operation of the routing zone controller is to define the order of the nodes or end points of each path segments to be routed ....; See: Col. 5 par [0067]);

means for adjusting within said proposed physical layout said initial array of nodes (such as…*intermediate or target nodes which are virtual nodes assigned…such a virtual nodes or targets could be used to specify the location of a connection…a virtual node or target may be temporary and it may be movable during a routing analysis...*; See: [0112] lines 5-14), said means for adjusting including locating a particular number of nodes between a pair of said obstacles, said particular number corresponding to a maximum number of traces that can pass between said obstacles, each of said nodes positioned between said pair of said obstacles representing a possible location of one of said traces that can pass between said obstacles (such as *…the zone quanta concept enables both the analysis and the actual routing to take place in a defined zone quanta of limited area, wherein the number of routing path segments to be processed and the number of obstacles to routing the path segments are reduced...*; See: Col. 16 par [00157] lines 8-13); and

means for selecting a path through said adjusted array of nodes resulting in creation of a trace that passes between said pair of obstacles in said proposed physical layout (for example, *Fig. 5 selecting the shorts sum of possible path that connect the three nodes 230-234, therefore in this case the selected path which is the shortest of all is segments C1 and C2, which provides the shortest overall length of the path that connects nodes 230, 232, and 234*; See: Col. 8 par [0113], [0114], Figs. 5 and 6).

Vaughn et al fails expressly to disclose means for receiving information representing a proposed physical layout of a routing space of an electronics system including locations of obstacles within said proposed physical layout.

Chapman et al discloses means for receiving information representing a proposed physical layout of a routing space of an electronics system including locations of obstacles within said proposed physical layout (such as *…a data representation of the integrated circuit and connection data are received, the data representation specifies the devices and cells contained in the integrated circuit….*; See: Col. 7 lines 24-40, Fig. 4A #404, and #406).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Chapman et al with Vaughn et al because both references are clearly concerned with routing an integrated circuit. The motivation for doing so would have been convenient to receive information of the integrated circuit layout to satisfy specified design criteria.

22. As per Claim 3, Vaughn et al discloses the computer system of claim 2, wherein said means for adjusting comprises, determining means for determining said particular number of paths traces that may pass between said pair of obstacles (such as *…the zone quanta concept enables both the analysis and the actual routing to take place in a defined zone quanta of limited area, wherein the number of routing path segments to be processed and the number of obstacles to routing the path segments are reduced...*; See: Col. 16 par [00157] lines 8-13).

23. As per Claims 4 and 5, Canceled.

24. As per Claim 6, Vaughn et al discloses the computer system of claim 2, wherein said means for adjusting locates said particular number of nodes along a line segment between said pair of obstacles (such as *…the zone quanta concept enables both the analysis and the actual routing to take place in a defined zone quanta of limited area, wherein the number of routing path segments to be processed and the number of obstacles to routing the path segments are reduced...*; See: Col. 16 par [00157] lines 8-13).

25. As per Claim 7, Vaughn et al discloses the computer system of claim 6, wherein said line segment is a shortest line segment between said pair of obstacles (See: Col. 6 par [0104]).

26. As per Claim 8, Vaughn et al discloses the computer system of claim 2, wherein said means for adjusting adjusts a location of each of at least one of said nodes in accordance with a proximity of said node to an object in said routing space (such as…*intermediate or target nodes which are virtual nodes assigned…such a virtual nodes or targets could be used to specify the location of a connection…a virtual node or target may be temporary and it may be movable during a routing analysis...*; See: [0112] lines 5-14).

27. As per Claim 9, Vaughn et al discloses the computer system of claim 2 further comprising means for linking said adjusted initial array of nodes (See: Fig. 6).

28. As per Claim 10, Vaughn et al discloses the computer system of claim 9, wherein said means for linking creates a link between each node in said array and nodes within

a predetermined proximity of said each node without crossing any of said links (See: Fig. 5 and Fig. 6).

29. As per Claim 11, Vaughn et al discloses the computer system of claim 10, wherein said path traverses ones of said links (See: [0163] lines 10-15).

30. As per Claim 12, Vaughn et al discloses a computer comprising computer hardware system for use in generating paths finding a path for electrically conductive traces within a routing space comprising:

means for providing an array of linked nodes within said proposed physical layout of said routing space, said array including a source node, a destination node, and a plurality of intermediate nodes (such as *...start node, interim node and target node...*; See: [0184], Fig. 5 and Fig. 6); and

means for determining a path from said source node to said destination node through said linked nodes resulting in creation of a trace from said source node to said destination node in said proposed physical layout (See: Fig. 5 and Fig. 6 and corresponding texts), wherein said means for determining comprises:

means for iteratively creating a plurality of partial paths, each said partial path extending from said source node to an intermediate node in said array (See: [0180], Fig. 6 and corresponding texts);

means for determining a routing cost of each said partial path (such as *...selecting the shortest path...*; See: [0104]); and

means for discarding all of said partial paths that extend to one intermediate node except the partial path with the lowest routing cost if more than one partial path

extends to said one intermediate node (such as *...selecting the shortest path...*; See: [0104]).

Vaughn et al fails expressly to disclose means for receiving information representing a proposed physical layout of a routing space of an electronics system.

Chapman et al discloses means for receiving information representing a proposed physical layout of a routing space of an electronics system (such as *…a data representation of the integrated circuit and connection data are received, the data representation specifies the devices and cells contained in the integrated circuit….*; See: Col. 7 lines 24-40, Fig. 4A #404, and #406).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Chapman et al with Vaughn et al because both references are clearly concerned with routing an integrated circuit. The motivation for doing so would have been convenient to receive information of the integrated circuit layout to satisfy specified design criteria.

31. As per Claim 13, Vaughn et al discloses the computer system of claim 12, wherein said means for iteratively creating creates said plurality of partial paths by creating initial paths from said source node to first nodes linked to said source node (See: Fig. 6, Fig. 14G and corresponding texts).

32. As per Claim 14, Vaughn et al discloses the computer system of claim 13, wherein said means for iteratively creating creates said plurality of partial paths further by extending said initial paths from said first nodes to nodes linked to said first nodes. (See: Fig. 6, Fig. Fig. 14F, 14G and corresponding texts).

33. As per Claim 15, Vaughn et al discloses the computer system of claim 12, wherein said means for providing further comprises means for creating for each node in said array a link between said each node and nodes within a predetermined proximity of said each node without crossing any of said links (See: Fig. 6, Fig. Fig. 14F, 14G and corresponding texts).

34. As per Claim 16, Vaughn et al discloses the computer system of claim 12, wherein said means for providing further comprises means for creating for each node in said array shortest links between said each node and nodes within a predetermined proximity of said each node without crossing any of said links (See: [0104] lines 1-9).

35. As per Claim 17, Vaughn et al discloses the computer system of claim 12, wherein said means for providing further comprises: means for selecting one of said nodes of said array; means for creating a link to another node of said array that is within a predetermined distance of said selected node; and means for deleting, if said created link crosses another link, a longest of said crossed links (See: Col. 8 par [0113]).

36. As per Claim 18, Vaughn et al discloses a computer comprising computer hardware for use in generating paths for electrically conductive traces within a routing space system comprising:

means for creating an initial array of nodes within said proposed physical layout of said routing space (such as …the routing path data from the optimized segments file created by the analysis engine and redefines the path segments in terms of coordinates ...the end result of the operation of the routing zone controller is to define the order of the nodes or end points of each path segments to be routed ....; See: Col. 5 par [0067]);

means for applying forces to ones of said nodes, wherein a magnitude of one of said forces applied to one of said nodes is proportional to a proximity of said one of said nodes to one of said obstacles (such as *…virtual node or target may movable during routing analysis* (See: par [0112]*)…nodes locate points along the routing surface in which the path segment is jogged or changed in direction to bypass the obstacle* (see: par [0182]);

means for moving within said proposed physical layout each of said ones of said nodes in accordance with said force applied to said one of said nodes (such as…intermediate or target nodes which are virtual nodes assigned…such a virtual nodes or targets could be used to specify the location of a connection…a virtual node or target may be temporary and it may be movable during a routing analysis...; See: [0112] lines 5-14); and

means for selecting a path through said adjusted array of nodes resulting in creation of a trace that passes through at least one of said nodes moved by said means for moving (for example, Fig. 5 selecting the shorts sum of possible path that connect the three nodes 230-234, therefore in this case the selected path which is the shortest of all is segments C1 and C2, which provides the shortest overall length of the path that connects nodes 230, 232, and 234; See: Col. 8 par [0113], [0114], Figs. 5 and 6).

Vaughn et al fails expressly to disclose means for receiving information representing a proposed physical layout of a routing space of an electronics system.

Chapman et al discloses means for receiving information representing a proposed physical layout of a routing space of an electronics system (such as …a data

representation of the integrated circuit and connection data are received, the data representation specifies the devices and cells contained in the integrated circuit….; See: Col. 7 lines 24-40, Fig. 4A #404, and #406).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Chapman et al with Vaughn et al because both references are clearly concerned with routing an integrated circuit. The motivation for doing so would have been convenient to receive information of the integrated circuit layout to satisfy specified design criteria.

37. As per Claims 19, and 20, Canceled.

38. As per Claim 21, The computer system of claim 18, wherein said means for applying a plurality of forces to one of said nodes, wherein a magnitude of each of said plurality of forces corresponds to a proximity of said node to one of said plurality of obstacles (such as *…virtual node or target may movable during routing analysis* (See: par [0112]*)…nodes locate points along the routing surface in which the path segment is jogged or changed in direction to bypass the obstacle* (see: par [0182]); and

said means for moving moves one of said nodes in accordance with a vector sum of said plurality of forces applied to said one of said nodes (such as…a virtual node or target may be temporary and it may be movable during a routing analysis...; See: [0112] lines 5-14).

39. As per Claims 22-43, Canceled.

40. As per Claim 44, Vaughn et al discloses the computer system of claim 2, wherein said path is stored within said system compute (such as *system database 106*).

41. As per Claim 45, canceled.

42. As per Claim 46, the instant claims recite substantially same limitation as the above rejected claim 44, and therefore rejected under the same rationale.

43. As per Claim 47, Canceled.

44. As per Claim 48, the instant claims recite substantially same limitation as the above rejected claim 44, and therefore rejected under the same rationale.

45. As per Claims 49-54, Canceled.

46. As per claim 55, Vaughn et al discloses the computer system of claim 2, wherein said means for creating an initial array of nodes creates the initial array of nodes in a honeycombed pattern (See: Fig. 10B #366).

47. As per Claim 56, Vaughn et al discloses the computer system of claim 2, wherein said means for creating an initial array of nodes creates the initial array of nodes wherein a random location of at least one node is generated (such as…a virtual node or target may be temporary and it may be movable during a routing analysis...; See: [0112] lines 5-14).

48. As per Claim 57, the instant claims recite substantially same limitation as the above rejected claim 55, and therefore rejected under the same rationale.

49. As per Claim 58, the instant claims recite substantially same limitation as the above rejected claim 56, and therefore rejected under the same rationale.

50. As per Claims 59-62, Canceled.

51. As per Claim 63, Vaughn et al discloses the computer of claim 12, wherein said means for determining a routing cost determines said routing cost of each said partial

path by summing a length of said partial path and a length of a straight line from said intermediate node to which said partial path extends to said destination node (such as…*the circuit paths must kept to a minimum in order to keep the cost of reproducing the circuit within reasonable limits…*(See: Col. 1 par [0002] lines 12-15) ...then ...*selecting the shortest path connecting all five nodes...*; See: Col. 6 par [0104]).

Conclusion

52. All claims are rejected.

53. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Examiner Remarks

54. Examiner's Note: **Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant.**

Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. **It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.**

Examiner Request

55. **In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on** for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

MPEP states:

"…with respect to newly added or amended claims, applicant should show support in the original disclosure for the new or amended claims. See MPEP § 714.02 and § 2163.06."

Requests for Interview

56. In accordance with 37 CFR 1.133(a)(3), requests for interview must be made in advance. Interview requests are to be made by telephone (571-272-8571) or FAX (571-273-8571). Applicants must provide a detailed agenda as to what will be discussed (generic statement such as "discuss §102 rejection" or "discuss rejections of claims 1-3" may be denied interview). The detail agenda along with any proposed amendments is to be written on a PTOL-413A or a custom form and should be faxed (or emailed, subject to MPEP 713.01.I / MPEP 502.03) to the Examiner at least 3 days prior to the

scheduled interview. Interview requests submitted within amendments may be denied because the Examiner was not notified, in advance, of the Applicant Initiated Interview Request and due to time constraints may not be able to review the interview request to prior to the mailing of the next Office Action.

Communications

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is 571-272-8571. The examiner can normally be reached on 8:00 am - 4:30 pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kibrom K Gebresilassie/
Examiner, Art Unit 2128

/Hugh Jones/

Primary Examiner, Art Unit 2128